operation control signal EN and may analyze the first power sequence PSEQ**1**, the second power sequence PSEQ**2**, and the operation control signal EN in operation S**110**. According to the analysis result, the voltage regulator **130** may select the level of the gate voltage VG supplied to the gate **303** of the power transistor **600** and the level of the body voltage VB supplied to the body **601** of the power transistor **600**, as described above with reference to FIGS. **1** through **10**, in operation S**120**.

[0135] As described above, according to an exemplary embodiment of the inventive concept, a voltage regulator using multi-power and gain-boosting techniques boosts the gain of an error amplifier included in the voltage regulator using the gain-boosting technique, so that the voltage regulator operates normally even when a dropout voltage is very low. As a result, the voltage regulator increases or maximizes its power efficiency. In addition, when an electronic device includes the voltage regulator, the use time of a battery of the electronic device is increased and the outflow of energy due to power loss is prevented, which reduces heat generated in the electronic device.

[0136] While the inventive concept has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in forms and details may be made therein without departing from the spirit and scope of the inventive concept as defined by the following claims.

1. A voltage regulator, comprising:

an error amplifier configured to receive a first voltage through a first node as an operating voltage, to amplify a difference between a reference voltage and a feedback voltage, and to output an amplified voltage;

a power transistor connected between a second node through which a second voltage is supplied and an output node; and

a switch circuit configured to select a level of a gate voltage supplied to a gate of the power transistor and a level of a body voltage supplied to a body of the power transistor in response to a first power sequence of the first voltage, a second power sequence of the second voltage, and an operation control signal.

2. The voltage regulator of claim **1**, wherein the first voltage is higher than the second voltage.

3. The voltage regulator of claim **1**, wherein when one of the first and second voltages is not powered up, the switch circuit selects a higher one of the first voltage and the second voltage as the gate voltage and the body voltage and disconnects the gate of the power transistor from an output node of the error amplifier.

4. The voltage regulator of claim **1**, wherein when both of the first and second voltages are powered up and the operation control signal is disabled, the switch circuit selects the first voltage or second voltage as the gate voltage and the body voltage and connects the gate of the power transistor to an output node of the error amplifier.

5. The voltage regulator of claim **1**, wherein when both of the first and second voltages are powered up and the operation control signal is enabled, the switch circuit selects an output voltage of the error amplifier as the gate voltage and the second voltage as the body voltage.

6. The voltage regulator of claim **5**, wherein the error amplifier outputs the amplified voltage using the first voltage as the operating voltage when the operation control signal is enabled and does not use the first voltage as the operating voltage when the operation control signal is disabled.

7. The voltage regulator of claim **1**, wherein the switch circuit comprises:

a first switch circuit connected between an output node of the error amplifier and the gate of the power transistor;

a second switch circuit connected to the first node, the second node, and the gate of the power transistor; and

a third switch circuit connected to the first node, the second node, and the body of the power transistor.

8. The voltage regulator of claim **7**, wherein the first switch circuit controls a connection between the output node of the error amplifier and the gate of the power transistor in response to a power-on signal generated in response to the first power sequence and the second power sequence,

the second switch circuit controls a connection between the first node and the gate of the power transistor and a connection between the second node and the gate of the power transistor in response to the power-on signal and the operation control signal, and

the third switch circuit controls a connection between either of the first and second nodes and the body of the power transistor in response to the power-on signal and the operation control signal.

9. The voltage regulator of claim **8**, wherein each of the first through third switch circuits comprises a logic gate circuit configured to process at least one signal among the power-on signal and the operation control signal and the logic gate circuit uses a higher one of the first voltage and the second voltage as an operating voltage.

10. The voltage regulator of claim **1**, wherein the error amplifier comprises:

an amplifier stage having a two-stage cascode architecture and configured to amplify the difference between the reference voltage and the feedback voltage; and

an output stage having the two-stage cascode architecture and configured to output the amplified voltage from the amplifier stage to the switch circuit.

11. The voltage regulator of claim **10**, wherein the output stage comprises:

a first feedback loop disposed at a pull-up path between the first node and an output node of the error amplifier; and

a second feedback loop disposed at a pull-down path between the output node of the error amplifier and a ground.

12. The voltage regulator of claim **11**, wherein the error amplifier further comprises a third feedback loop disposed between the output node of the error amplifier and the ground and shares a part of the second feedback loop.

13. A mobile device, comprising:

a voltage regulator; and

a power management integrated circuit configured to supply a first voltage to the voltage regulator through a first transmission line and to supply a second voltage to the voltage regulator through a second transmission line,

wherein the voltage regulator comprises:

an error amplifier configured to receive the first voltage through a first node connected to the first transmission line as an operating voltage, to amplify a difference between a reference voltage and a feedback voltage, and to output an amplified voltage;